PRELIMINARY AMENDMENT

Please amend the above-referenced patent application as follows:

In the Claims:

Please amend claims 41 and 65. The claims are as follows:

1-27. (Withdrawn)

28. (Original) An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2; and

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure.

29. (Original) The electrical structure of claim 28, wherein the first multilevel conductive via is a stacked via.

30. (Original) The electrical structure of claim 28, wherein the first multilevel conductive via is a deep via.

31. (Original) The electrical structure of claim 28, wherein the first multilevel conductive via is a simple-deep via

32. (Original) The electrical structure of claim 28, wherein the first multilevel conductive via is a stacked-deep via.

33. (Original) The electrical structure of claim 28, wherein the CPS substructure is a single CPS substructure.

34. (Original) The electrical structure of claim 28, wherein the CPS substructure is a double CPS substructure.

35. (Original) The electrical structure of claim 28, wherein N=2.

36. (Original) The electrical structure of claim 28, further comprising a second multilevel conductive via through the DM laminate, wherein the second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure.

A1

37. (Original) The electrical structure of claim 28, wherein the first metal layer is at the first

external surface of the CPS substructure.

38. (Original) The electrical structure of claim 28, further comprising a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure, and wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via.

39. (Original) The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is within an interior of the CPS substructure.

40. (Original) The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is a complex power-signal of the CPS substructure.

41. (Currently Amended) The electrical structure of claim 38, wherein the fraction is equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, and wherein the first metal layer is at the second external surface.

A1

42. (Original) An electrical structure, comprising:

a complex power-signal (CPS) substructure that has satisfied an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure; and

a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure.

43. (Original) The electrical structure of claim 42, wherein M=N.

44. (Original) The electrical structure of claim 42, further comprising a conductive through hole through a total thickness of the electrical structure, including through the first DM laminate, the CPS substructure, and the second DM laminate.

A1

45. (Original) An electrical structure, comprising:

a composite complex power-signal (CPS) substructure that includes an interfacing dielectric layer sandwiched between a first CPS substructure and a second CPS substructure, wherein a first surface of the first CPS substructure is coupled to a first surface of the interfacing dielectric layer, and wherein a first surface of the second CPS substructure is coupled to a second

surface of the interfacing dielectric layer,

said first CPS substructure having passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance, and

said second CPS substructure having passed the electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance,

A1

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a second surface of the first CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a metal layer of the first CPS substructure; and

a second DM laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second surface of the second CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a metal layer of the second CPS substructure.

46. (Original) The electrical structure of claim 45, wherein M=N.

47. (Original) The electrical structure of claim 45, further a conductive through hole through a total thickness of the electrical structure, including through the first DM laminate, the composite CPS substructure, and the second DM laminate.

48. (Original) An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2;

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure; and

a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure.

49. (Original) An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical

open, and erroneous an impedance;

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure;

a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure; and

a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure.

A1

50. (Original) An electrical structure, comprising:

a composite complex power-signal (CPS) substructure that includes an interfacing dielectric layer sandwiched between a first CPS substructure and a second CPS substructure, wherein a first surface of the first CPS substructure is coupled to a first surface of the interfacing dielectric layer, and wherein a first surface of the second CPS substructure is coupled to a second surface of the interfacing dielectric layer,

said first CPS substructure having passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the

test for electrical integrity includes a test for at least one of an electrical short, electrical open, and erroneous impedance, and

said second CPS substructure having passed the electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance,

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a second surface of the first CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a metal layer of the first CPS substructure;

a second DM laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second surface of the second CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a metal layer of the second CPS substructure; and

a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the first CPS substructure.

51. (Original) An electrical structure, comprising:

a complex power-signal (CPS) substructure;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal

A1

number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2; and

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure.

52. (Original) The electrical structure of claim 51, wherein the first multilevel conductive via is a stacked via.

53. (Original) The electrical structure of claim 51, wherein the first multilevel conductive via is a deep via.

54. (Original) The electrical structure of claim 51, wherein the first multilevel conductive via is a simple-deep via

55. (Original) The electrical structure of claim 51, wherein the first multilevel conductive via is a stacked-deep via.

56. (Original) The electrical structure of claim 51, wherein the CPS substructure is a single CPS substructure.

57. (Original) The electrical structure of claim 51, wherein the CPS substructure is a double CPS

substructure.

58. (Original) The electrical structure of claim 51, wherein N=2.

59. (Original) The electrical structure of claim 51, further comprising a second multilevel conductive via through the DM laminate, wherein the second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure.

60. (Original) The electrical structure of claim 51, wherein the first metal layer is at the first external surface of the CPS substructure.

61. (Original) The electrical structure of claim 51, further comprising a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure, and wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via.

62. (Original) The electrical structure of claim 51, wherein the fraction is less than 1, and wherein the first metal layer is within an interior of the CPS substructure.

63. (Original) The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is a complex power-signal of the CPS substructure.

64. (Original) The electrical structure of claim 38, wherein the fraction is equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, and wherein first metal layer is at the second external surface.

65. (Currently Amended) The ~~method~~ electrical structure of claim 38, further comprising a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure.

A1 Concluded